25ECMJ205: Digital System Design

w. e. f. Academic Year:	**2026-27**
Semester:	**3**
Category of the Course:	**Program Core Course** (PCC).
Prerequisite:	A solid foundation in Mathematics, Physics & basic Electronic principles is essential for understanding Boolean algebra, logic gates & design of digital circuits.
Rationale:	Digital Logic Design teaches fundamental digital circuits, Boolean algebra, combinational and sequential systems, enabling students to analyze, design & simulates efficient digital systems, forming a foundation for advanced Electronics and Communication engineering.

Course Outcomes:
After Completion of the Course, Student will able to:

	Course Outcome (CO)	**RBT Level (Cognitive Domain)**	**Marks % Weightage (Approx.)**
CO1	Apply number systems, Boolean algebra, and logic gates to solve digital logic problems.	L3 (Apply)	20%
CO2	Analyze and design combinational logic circuits such as adders, subtractors, multiplexers, and decoders.	L4 (Analyze)	20%
CO3	Analyze the behavior of sequential logic circuits using flip-flops and state diagrams.	L4 (Analyze)	20%
CO4	Apply the concept of registers and shift registers for data storage and data transfer operations.	L3 (Apply)	20%
CO5	Design and analyze different types of counters including synchronous and asynchronous counters.	L4 (Analyze)	20%

Teaching and Evaluation Scheme:

Teaching Scheme					**Examination Scheme**				
L	**T**	**P**	**C**	**Hrs/Week**	**IE**	**Theory**	**CIA**	**Practical**	**Total Marks**
2	0	4	4	6	40	60	30	20	150

IE: Internal Evaluation
CIA: Continuous Internal Assessment
Theory: Theory Exam (End Semester)
Practical: Practical Exam (End Semester)

Detailed Syllabus:

Topic		Hrs.	% of Weightage (Approx.)
UNIT: 1	**Boolean Algebra, Boolean Functions and logic gates:**	**8**	**20%**
Binary System, number conversion, Boolean Algebra, Standard Representation of Logical Functions, Digital Logic Gates, Universal Gate, Min-term And Max-term, Karnaugh map method.			
UNIT: 2	**Combinational Logic Circuits:**	**6**	**20%**
Introduction to combinational logic circuits, Half Adder, full Adder, half subtractor, full subtractor, Multiplexer and Decoder.			
UNIT: 3	**Sequential Logic Circuits:**	**6**	**20%**
Introduction to sequential logic circuits, Flip-Flops, Clocked Sequential Circuits, Flip-Flop Excitation Tables with State Diagram.			
UNIT: 4	**Registers:**	**5**	**20%**
Introduction to register, types of Registers, Introduction to Shift Registers. Serial and parallel shift operation in Registers.			
UNIT: 5	**Counters:**	**5**	**20%**
Introduction to counters, Binary Counter, Ripple Counter, Synchronous Counter and Asynchronous Counter.			
		30	**100%**

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks in Percentage					
Remember	Understand	Apply	Analyze	Evaluate	Create
-	-	40	60	-	-

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

List of Practical:

Topic	Hrs
1. To Study & verify the Truth tables of Digital logic Gates.	2
2. To study and verify various theorems of Boolean ALGEBRA including De Morgan's.	2
3. To Study and Perform the Functionality of NAND and NOR gate as Universal Gate.	2
4. To develop ADDER and verify its operation.	2
5. To develop SUBTRACTOR and verify its operation.	2
6. To verify the operation of 2 to 4 line Decoder and 3 to 8 line Decoder using IC-74138	2
7. To study and verify the Truth table of 4:1 MUX & 8:1 Multiplexer using IC	4

74151A.	
8. To verify the operation of a 1 bit Comparator & 4-bit comparator using IC 7485.	4
9. To study & perform PARITY GENERATOR/CHECKER.	2
10. To test the seven segments display using 7447 IC.	2
11. To study & verify the Truth tables of Different types of Flip-Flops. - R-S (Reset-Set) flip-flop - Clocked R-S flip-flop.	4
12. To study & verify the Truth tables of Different types of Flip-Flops - D (Delay)flip-flop - Clocked D flip-flop.	4
13. To study & verify the Truth tables of Different types of Flip-Flops. - J-K flip-flop - T (Toggle) flip-flop.	4
14. To simulate Digital Logic Gates using a simulation Tool.	4
15. To simulate NAND and NOR gates as Universal Gates using a Simulation tool.	4
16. To simulate ADDER using a Simulation tool.	4
17. To simulate Subtractor using a Simulation tool.	4
18. To simulate a Boolean Algebra using a Simulation Tool.	4
19. Mini Project based on Digital Electronics	4
TOTAL	**60**

TEXT/REFERENCE BOOKS:

TEXT BOOKS:

1. M. Morris Mano- Digital logic and computer Design, PHI.
2. A. Anand Kumar- Fundamentals of Digital Circuits, PHI.
3. Douglas Perry, " VHDL" , McGraw Hill, 4th edition, 2002

REFERENCE BOOKS:

1. R.P.Jain- Digital Electronics, McGraw Hill
2. B. Somanathan Nair- Digital Electronics and Logic Design, PHI

Teaching Learning Method:

- Lecture-Based Teaching-Learning
- Problem-Solving Method
- Collaborative Method
- Problem-Based Learning
- Mini Projects / Application-Based Learning

Course Outcomes Mapping:

CO	Course Outcome (CO)	POs/PSOs Mapped	Cognitive Level (RBT)	Knowledge Category	Class Session (Lecture)
CO1	Apply number systems,	PO1, PO2,	L3 (Apply)	Conceptual,	8

	Boolean algebra, and logic gates to solve digital logic problems.	PSO1		Procedural	
CO2	Analyze and design combinational logic circuits such as adders, subtractors, multiplexers, and decoders.	PO2, PO3, PO5, PSO1, PSO2	L4 (Analyze)	Conceptual, Procedural	6
CO3	Analyze the behavior of sequential logic circuits using flip-flops and state diagrams.	PO1, PO2, PO4, PSO1	L4 (Analyze)	Conceptual	6
CO4	Apply the concept of registers and shift registers for data storage and data transfer operations.	PO1, PO5, PSO2	L3 (Apply)	Procedural	5
CO5	Design and analyze different types of counters including synchronous and asynchronous counters.	PO2, PO3, PO5, PSO1, PSO2	L4 (Analyze)	Conceptual, Procedural	5

Mapping of COs with POs & PSOs:

CO	PO											PSO	
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**1**	**2**
CO1	3	3	0	0	0	0	0	0	0	0	0	3	0
CO2	0	3	2	0	3	0	0	0	0	0	0	3	3
CO3	3	3	0	1	0	0	0	0	0	0	0	3	0
CO4	3	0	0	0	3	0	0	0	0	0	0	0	3
CO5	0	3	2	0	3	0	0	0	0	0	0	3	3

3: High, 2: Medium, 1: Low

Sustainable Development Goals (SDG) Integration:

The course on Digital System Design contributes to SDG 4 (Quality Education) by strengthening students' foundational and analytical skills in digital electronics. It supports SDG 9 (Industry, Innovation and Infrastructure) by enabling the design and development of efficient digital systems used in modern technology. Additionally, it aligns with SDG 7 (Affordable and Clean Energy) through the promotion of optimized, low-power digital circuits. Overall, the course prepares students for innovation-driven and sustainable technological development.

SDG Mapping with Course Outcomes:

CO	Course Outcome	Relevant SDGs	Justification
CO1	Apply number systems, Boolean algebra, and logic gates to solve digital logic problems.	SDG 4, SDG 9	Builds strong foundational knowledge in digital systems, promoting technical education and innovation skills necessary for modern industries.
CO2	Analyze and design combinational logic circuits such as adders, subtractors, multiplexers, and decoders.	SDG 9, SDG 8	Enables students to design efficient digital systems used in computing and communication industries, contributing to technological advancement and employability.
CO3	Analyze the behavior of sequential logic circuits using flip-flops and state diagrams.	SDG 9	Sequential circuit design is essential in automation, embedded systems, and digital devices, supporting innovation in industrial infrastructure.
CO4	Apply the concept of registers and shift registers for data storage and data transfer operations.	SDG9, SDG 7	Efficient data storage and transfer techniques contribute to optimized digital systems, reducing power consumption in electronic devices.
CO5	Design and analyze different types of counters including synchronous and asynchronous counters.	SDG 9, SDG 11	Counters are fundamental in digital control systems used in smart infrastructure, traffic systems, and automation, supporting sustainable urban development.