Kadi Sarva Vishwavidyalaya

Faculty of Engineering & Technology

Second Year Bachelor of EC Engineering

Subject Code: EC305 -N	Subject Title: DIGITAL SYSTEM DESIGN

Course Objective:

- To present a problem oriented introductory knowledge of Digital Electronics.
- To address the underlying concepts and methods behind Digital Logic Design

Teaching Scheme (Credits and Hours)

Teaching scheme				Total Credit	Evaluation Scheme					
L	T	P	Total		Theory		IE Marks	CIA Marks	Pract. Marks	Total Marks
Hrs	Hrs	Hrs	Hrs		Hrs	Marks				
03	00	02	05	04	03	70	30	20	30	150

Outline of the Course:

Sr. No.	Title of the Unit	Hours
1	Boolean Algebra and logic gates	8
2	Simplification of Boolean Functions	8
3	Combinational Logic Circuits With MSI AND LSI	8
4	Sequential Logic Circuits	7
5	Registers, Counters and the Memory unit	7
6	Logic Families	4
7	Finite State Machine(FSM)	6

Total hours (Theory): 48

Total hours (Tutorial): 32

Total hours: 80

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Detailed Syllabus:

Unit No.	Topic	Lecture Hours	Weightage(%)
1.	**Boolean Algebra and Logic Gates : Binary System, number conversion,** Basic Definition, Basic Theorem and Properties of Boolean Algebra, Standard Representation of Logical Functions, Universal Gate, Min-term And Max-term, Logic Operations, Digital Logic Gates	**8**	**18**
2.	**Simplification of Boolean Functions:** Different types Map method, Product of sum Simplification, NAND or NOR implementation, Don't Care condition, Tabulation method	**8**	**18**
3.	**Combinational Logic Circuits With MSI AND LSI:** Introduction, Design Procedure, adder, subtractor, Parity checker Parity Generator, Code Conversion. Decoder, Multiplexer	**8**	**14**
4.	**Sequential Logic Circuits:** Introduction, Flip-Flops, Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Flip-Flop Excitation Tables, Design Procedure, Design of Counters	**7**	**17**
5.	**Registers, Counters and the Memory unit:** Introduction, Registers, Shift Registers, Ripple Counters, Synchronous Counters.	**7**	**16**
6.	**Logic Families :** Digital IC specification terminology, Logic families, Comparison of CMOS and TTL families	**4**	**5**
7.	**Finite State Machine:** Synchronous Sequential Circuits Design using FSM (Melay and Moore Model).State Diagram, State Table, State Assignment, Rules for state Assignment, Design Procedure, Asynchronous Sequential Circuits Design, application and Analysis Asynchronous Sequential of machines	**6**	**12**
	Total	**48**	**100**

Instructional Method and Pedagogy (Continuous Internal Assessment (CIA) Scheme)

- At the start of course, the course delivery pattern , prerequisite of the subject will be discussed
- Lecture may be conducted with the aid of multi-media projector, black board, OHP etc. & equal weightage should be given to all topics while teaching and conduction of all examinations.
- Attendance is compulsory in lectures and laboratory, which may carries five marks in overall evaluation.
- One/Two internal exams may be conducted and total/average/best of the same may be converted to equivalent of 30 marks as a part of internal theory evaluation.
- Assignment based on course content will be given to the student for each unit/topic and will be evaluated at regular interval. It may carry an importance of ten marks in the overall internal evaluation.
- Surprise tests/Quizzes/Seminar/Tutorial may be conducted and having share of five marks in the overall internal evaluation.

Learning Outcomes:

At the end of this course, the student would be able

The student can identify different areas of Digital circuits. Can find the applications of all the areas in day to day life. Can identify the operations, working, construction, material etc. aspects of Digital devices, ICs, Logic Gates etc.

TEXT BOOKS:

1. M. Morris Mano- Digital logic and computer Design, PHI
2. A. Anand Kumar- Fundamentals of Digital Circuits, PHI
3. Douglas Perry, " VHDL" , McGraw Hill, 4th edition, 2002

REFERENCE BOOKS:

1. R.P.Jain- Digital Electronics, McGraw Hill
2. B. Somanathan Nair- Digital Electronics and Logic Design, PHI

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LIST OF EXPERIMENTS

Sr. No.	Experiment Title
1.	To Study & verify the Truth tables of Digital logic Gates.
2.	To study and verify various theorems of Boolean ALGEBRA including De-Morgan's.
3.	To Study and Perform the Functionality of NAND and NOR gate as Universal Gate.
4.	To develop ADDER and SUBTRACTOR and verify its operation.
5.	To verify the operation OF DECODER - 2 to 4 line Decoder - 3 to 8 line Decoder using IC-74138
6.	To study and verify the Truth tables of 8:1 Multiplexer using IC 74151A.
7.	To verify the operation of 4-bit comparator using IC 7485.
8.	To study & perform PARITY GENRATOR/CHECKER.
9.	To test the seven segment display using 7447 IC.
10.	To study & verify the Truth tables of Different types of Flip-Flops. - R-S (Reset-Set) flip-flop - Clocked R-S flip-flop - D (Delay)flip-flop - Clocked D flip-flop - J-K flip-flop - T (Toggle) flip-flop
11.	Implementation of basic logic gates and its testing using MATLAB or LabVIEW
12.	Implementation of adder circuits and its testing using MATLAB or LabVIEW
13.	Implementation 4 to 1 multiplexer and its testing using MATLAB or LabVIEW
14.	Implementation of 3 to 8 decoder and its testing using MATLAB or LabVIEW
15.	Implementation of J-K and D Flip Flops and its testing using MATLAB or LabVIEW
16.	Implementation of sequential adder and its testing using MATLAB or LabVIEW
17.	Simulation of VHDL constructs and codes for combinational and sequential circuits.