Kadi Sarva Vishwavidyalaya

Faculty of Engineering & Technology

Electronics and communication Engineering

(Academic Year 2019-20)

Subject Code: EC 506-N	**Subject Title: VLSI TECHNOLOGY AND DESIGN**
Pre-requisite	

Course Objective:

The educational objectives of this course are

- Fundamentals of CMOS Digital VLSI design. Different Aspects of MOS inverters.
- MOS Logic circuits like combinational, sequential logic and dynamic logic circuits.
- FPGA & CPLD,VLSI Softwares: Xilinx, Simulation tool : Tanner.

Teaching Scheme (Credits and Hours)

Teaching scheme				**Total Credit**	**Evaluation Scheme**					**Total Marks**
L	**T**	**P**	**Total**		**Theory**		**IE Marks**	**CIA Marks**	**Pract. Marks**	
Hrs	**Hrs**	**Hrs**	**Hrs**		**Hrs**	**Marks**				
03	00	02	05	4	03	70	30	20	30	150

Outline Of the Course:

Sr. No	**Title of the Unit**	**Hours**
1.	Introduction	5
2.	Fabrication of MOSFET	5
3.	MOS Transistor	10
4.	MOS Inverters: Static Characteristics	5
5.	Combinational MOS Logic Circuits	5
6.	Sequential MOS Logic Circuits	6
7.	ASIC Design	6
8.	Programmable Logic Devices	6
		48

Total hours (Theory): 48
Total hours (Lab): 32
Total hours: 80

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Detailed Syllabus:

Sr. No.	Topic	Lecture Hours	Weightage(%)
1.	**Introduction**: Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality.	5	**10**
2.	**Fabrication of MOSFET:** Introduction, Fabrication Process flow, Basic steps, C-MOS n-Well Process.	5	**10**
3.	**MOS Transistor:** The Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure and Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling and small-geometry effects.	10	**15**
4.	**MOS Inverters: Static Characteristics:** Introduction, Resistive load Inverter, Inverter with n-type MOSFET load - Enhancement and Depletion type MOSFET load, CMOS Inverter.	5	**15**
5.	**Combinational MOS Logic Circuits**: Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logic circuits, Complex logic circuits.	5	**15**
6.	**Sequential MOS Logic Circuits**: Introduction, The SR latch circuit, Clocked latch and Flip-flop circuit, CMOS D-latch.	6	**15**
7.	**ASIC Design**: Introduction, Design Methodologies, Introduction to Hardware Description Language – VHDL, Structural, Behavioral and Data flow modeling.	6	**10**
8.	**Programmable Logic Devices**: Basics of Programmable Logic Devices, Architecture of CPLD & FPGA, Design and Implementation using CPLD and FPGA.	6	**10**
	Total	48	**100**

Instructional Method and Pedagogy:

- At the start of course, the course delivery pattern, prerequisite of the subject will be discussed.
- Lectures will be conducted with the aid of multi-media projector, black board, OHP etc.
- Attendance is compulsory in lecture and laboratory which carries 10 marks in overall evaluation.
- One internal exam will be conducted as a part of internal theory evaluation.
- Assignments based on the course content will be given to the students for each unit and will be evaluated at regular interval evaluation.
- Surprise tests/Quizzes/Seminar/tutorial will be conducted having a share of five marks in the overall internal evaluation.
- The course includes a laboratory, where students have an opportunity to build an appreciation for the concepts being taught in lectures.
- Experiments shall be performed in the laboratory related to course contents.

Learning Outcomes:

At the end of this course, the student would be able

- To differentiate the ideas and utilizations of VHDL Programming
- Learn significance of MOSFET and CMOS Fabrication with scaling
- Apply the concepts of Full-custom and semi-custom - FPGA.

TEXT BOOKS:

1. CMOS Digital Integrated circuits – Analysis and Design by Sung – Mo Kang, Yusuf Leblebici, TATA McGraw-Hill Pub. Company Ltd., Third Edition.
2. J. Bhasker, BHDL, Primer, Pearson Education Asia, Low Price Edition.

REFERENCE BOOKS:

1. Xilinx and Altera Application Notes on the architecture of FPGAs and CPLDs.
2. Basic VLSI Design By Pucknell and Eshraghian, PHI, 3rd ed.
3. D.Perry, BHDL, 2nd Ed., McGraw Hill International.
4. Introduction to VLSI Systems by Mead C and Conway, Addison Wesley
5. Introduction to VLSI Circuits & Systems – John P. Uyemura
6. Fundamentals of Digital Logic Design with VHDL, Brown and Vranesic

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List of experiments (Not limited to following. Subject teacher may modify the same)**:**

Sr. No.	Experiment Title
1.	Introduction to programmable devices (FPGA, CPLD)
2.	Introduction to Hardware Description Language (VHDL
3.	Introduction to the use programming tool.
4.	Implementation of basic logic gates and its testing.
5.	Implementation of adder circuits and its testing.
6.	Implementation of subtractor circuits and its testing.
7.	Implementation 8 to 1 multiplexer and its testing.
8.	Implementation of 3 to 8 decoder and its testing.
9.	Implementation of J-K and D Flip Flops and its testing.
10.	Implementation of sequential adder and its testing.
11.	Implementation of BCD counter and its testing.
12.	Implementation of two 8-bit MUX circuits and its testing.
13.	Implementation of any digital circuits using FSM.
14.	Simulation of CMOS Inverter using SPICE for transfer characteristic.
15.	VHDL based mini project