Kadi Sarva Vishwavidyalaya

Faculty of Engineering & Technology

Fourth Year Bachelor of EC Engineering

(VIIthsem Academic Year 2020)

Subject Code: EC704C-N	Subject Title: VLSI Testing & Verification

Course Objective:

- This course provides a platform for students to understand importance of testing, fundamental VLSI test principles, basic concepts of design of testability (DFT), logic simulation and fault simulation, and various techniques for test pattern generation etc.

Teaching scheme				Total Credit	EvaluationScheme					
					Theory		IE Marks	CIA Marks	Pract. Marks	Total Marks
L	T	P	Total							
Hrs	Hrs	Hrs	Hrs		Hrs	Marks				
04	00	02	06	05	03	70	30	20	30	150

Outline of the Course:

Sr. No.	TitleoftheUnit	Minimum Hours
1.	Introduction	**12**
2.	Design and Testability	**12**
3.	Logic and fault simulation	**12**
4.	Verification	**12**
5.	Functional verification	**12**
	Total	**60**

Total hours (Theory): 60
Total hours (Lab):
Total hours:

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Detailed Syllabus

Sr. No.	Topic	Lecture Hours	Weightage(%)
1.	**Introduction:** Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.	**12**	**15**
2.	**Design and Testability:** Introduction, Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special purpose Scan Designs, RTL Design for Testability	**12**	**30**
3.	**Logic and Fault Simulation:** Introduction, Simulation Models, Logic Simulation, Fault Simulation	**12**	**20**
4.	**Verification:** Importance of verification, Verification plan, Verification flow, Levels of verification, Verification methods and languages	**12**	**15**
5.	**Functional Verification:** Introduction to test bench, Test bench architecture, Types of test benches, case study	**12**	**20**
	Total	**60**	**100**

Instructional Method and Pedagogy:

- At the start of course, the course delivery pattern, prerequisite of the subject will be discussed.
- Lectures will be conducted with the aid of multi-media projector, black board, OHP etc.
- Attendance is compulsory in lecture and laboratory which carries 10 marks in overall evaluation.
- One internal exam will be conducted as a part of internal theory evaluation.
- Assignments based on the course content will be given to the students for each unit and will be evaluated at regular interval evaluation.
- Surprise tests/Quizzes/Seminar/tutorial will be conducted having a share of five marks in the overall internal evaluation.
- The course includes a laboratory, where students have an opportunity to build an appreciation for the concepts being taught in lectures.
- Experiments shall be performed in the laboratory related to course contents.

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Learning Outcome:

1) To realize importance and challenges of VLSI Testing at different abstraction levels.
2) To study and apply various fault models for generation of test vectors.
3) To calculate observability and controllability parameters of given circuit.
4) To study techniques to improve testability of a given circuit.
5) To convert a given circuit into a scan design.
6) To apply concepts of logic simulation and fault simulation in designing and testing of VLSI circuits.
7) To identify the different characteristics of verification, and apply different verification methods.

TEXT BOOKS:

1. VLSI Test Principles and Architectures, Wang Wu Wen, Morgan Kaufmann Publishers
2. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", M. Bushnell and V. D. Agrawal, Kluwer Academic Publishers, 2000
3. Digital Systems Testing and Testable Design, M. Abramovici, M. A. Breuer and A. D. Friedman, IEEE Press, 1990
4. Introduction to Formal Hardware Verification, T.Kropf, Springer Verlag, 2000
5. System-on-a-Chip Verification- Methodology and Techniques, P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001
6. Janick Bergeron, Writing Testbenches, Functional Verification of HDL Models, Springer

List of experiments (Not limited to following. Subject teacher may modify the same):

Sr. No.	Experiment Title
1.	To develop an exhaustive test bench for lower level combinational designs.
2.	To develop an exhaustive test bench for J-K flip-flop.
3.	To develop an exhaustive test bench for 4 bit up-down counter.
4.	Write a VHDL/Verilog code to realize functioning of Observation Point Insertion technique.
5.	Write a VHDL/Verilog code to realize functioning of control Point Insertion technique.
6.	Write a VHDL/Verilog code for MUX-D scan cell and Level Sensitive/edge triggered Muxed-D scan cell.
7.	Write a VHDL/verilog code to realize functioning of clocked scan cell and LSSD scan cell design.
8.	Write a VHDL/verilog code to realize functioning of LSSD double latch design.
9.	Write a VHDL/verilog code to realize functioning of Mixing negative-edge and positive-edge scan cell in a scan chain.
10.	Write a VHDL/verilog code to realize functioning of Linear feedback shift register.
11.	Write a VHDL/verilog code to realize functioning of built-in logic block obsrever.
12.	Write a VHDL/verilog code to realize functioning of Fixing bus contention in scan design rules.
13.	Write a VHDL/verilog code to realize functioning of Adding a lock-up latch between cross-clock-domain scan cells