Kadi Sarva Vishwavidyalaya

Faculty of Engineering & Technology

Second Year Bachelor of EE Engineering- Semester IV

With effect from: Academic Year 2018-19

EE407-N	**Digital Electronics**
Pre-requisite	

Teaching Scheme (Credits and Hours)

Teaching scheme				Total Credit	Evaluation Scheme					Total Marks
					Theory		IE Marks	CIA Marks	Pract. Marks	
L	T	P	Total							
Hrs	Hrs	Hrs	Hrs		Hrs	Marks				
03	00	02	05	04	03	70	30	20	30	150

Course Outcomes:

At the end of this course, students will demonstrate the ability to

- Understand working of logic families and logic gates.
- Design and implement Combinational and Sequential logic circuits.
- Be able to use PLDs to implement the given logical problem.

Outline of the Course:

Sr. No	Title of the Unit	Minimum Hours
1	Fundamentals of Digital Systems and Number system	8
2	Boolean Algebra and logic families:	8
3	Combinational Digital Circuits	8
4	Sequential circuits and systems	8
5	Semiconductor memories and Programmable logic devices	8
	Total	40

Total hours (Theory): 40
Total hours (Lab): 30
Total hours: 70

DETAILED SYLLABUS

Unit No	Topics	Lectures (Hours)	Weightage
1	**Fundamentals of Digital Systems and Number system** Digital signals, digital circuits,Binary, octal, hexadecimal and decimal Number systems and their inter conversion, BCD numbers (8421-2421), gray code, excess–3 code, cyclic code. Binary addition and subtraction, r's and (r-1)'s complement representation and their applications.	**8**	**20%**
2	**Boolean Algebra and logic families:** Logic gates (AND, OR, NOT, NAND, NOR, Ex-OR, Ex-NOR and their truth tables), Universal Gates, Laws of Boolean algebra, De-Morgan's theorem, Min term, Max term, POS, SOP, K-Map, don't care. Condition. Introduction to digital logic family such as RTL, DTL, TTL, ECL, CMOS and their comparative study, Basic circuit, performance characteristics, Wired logic, open collector output etc.	**8**	**20%**
3	**Combinational Digital Circuits:** Standard representation for logic functions, K-map representation, simplification oflogicfunctions using K-map, minimization of logical functions. Don't care conditions, Multiplexer,De-Multiplexer/Decoders, Adders, Subtractors, BCD arithmetic, carry look ahead adder,serialadder, ALU, elementary ALU design, popular MSI chips, digital comparator, paritychecker/generator, code converters, priority encoders, decoders.	**8**	**20%**
4	**Sequential circuits and systems:** A 1-bit memory, the circuit properties of Bistable latch, the clocked SR flip flop, J- K-T and D types flipflops, applications of flipflops, shift registers, applications of shift registers. Synchronous/Asynchronous counter operation, Up/down synchronous counter, Serial in/Serial out shift register, Serial in/parallel out shift register, parallel in/ parallel out shift register, parallel in/Serial out shift	**8**	**20%**

	register, Bi-directional register.		
5	**Semiconductor memories and Programmable logic devices.** Memory organization and operation, expanding memory size, classification and characteristics of memories, sequential memory, read only memory (ROM), read and write memory(RAM), content addressable memory (CAM), charge de coupled device memory (CCD), commonly used memory chips, ROM as a PLD, Programmable logic array, Programmable array logic, complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).	**8**	**20%**

INSTRUCTIONAL METHOD AND PEDAGOGY:

- At the start of course, the course delivery pattern , prerequisite of the subject will be discussed
- Lecture may be conducted with the aid of multi-media projector, black board, OHP etc. & equal weight age should be given to all topics while teaching and conduction of all examinations.
- Attendance is compulsory in lectures and laboratory, which may carries five marks in overall evaluation.
- One/Two internal exams may be conducted and total/average/best of the same may be converted to equivalent of 30 marks as a part of internal theory evaluation.
- Assignment based on course content will be given to the student for each unit/topic and will be evaluated at regular interval. It may carry an importance of ten marks in the overall internal evaluation.
- Surprise tests/Quizzes/Seminar/Tutorial may be conducted and having share of five marks in the overall internal evaluation.

LEARNING OUTCOME:

- The student can be acquired the basic knowledge of electric circuits, electrical fundamentals, thus being prepared to pursue any area of engineering spectrum in depth as desired.
- The students will be able to effectively employ electrical systems and lead the exploration of new applications and techniques for their use.

Text/References books:

1. R. P. Jain, "Modern Digital Electronics", McGraw Hill Education, 2009.

2. M. M. Mano, "Digital logic and Computer design", Pearson Education India, 2016.

3. A. Kumar, "Fundamentals of Digital Circuits", Prentice Hall India, 2016.

List of experiments:

Sr. No.	Name of experiment
1.	To Study & verify the Truth tables of various Digital logic Gates.
2.	To Study and verify various theorems of Boolean algebra.(like De-morgan's).
3.	To Study and perform the Functionality of NAND and NOR GATE as Universal Gate.
4.	To develop Adder and Subtractor digital logic circuit and verify its operation.
5.	To verify the operation of decoder(3x8).
6.	To verify the operation of multiplexer (4to1).
7.	To verify truth table of different Flip-Flops (SR,Jk,D,T).
8.	To study binary/BCD counter.
9.	To study shift registers.
10	Mini Model project using any digital logic circuits.